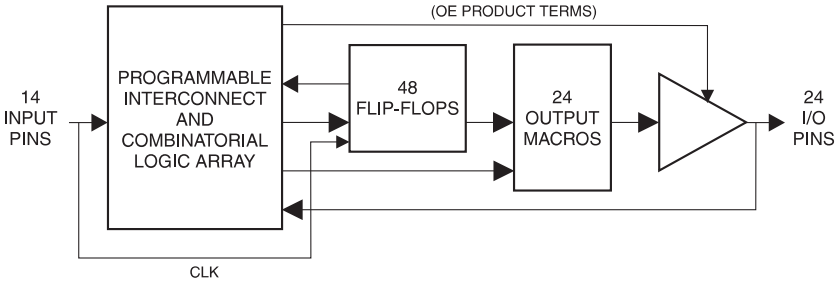
Features

- **High-performance, High-density, Electrically-erasable Programmable Logic Device**
- **Fully Connected Logic Array with 416 Product Terms**
- **10 ns Maximum Pin-to-pin Delay for 5V Operation**
- **Low-power Edge-sensing "L" Option with <1 mA Standby Current**
- **24 Flexible Output Macrocells**
  - **48 Flip-flops – Two per Macrocell**
  - **72 Sum Terms**
  - **All Flip-flops, I/O Pins Feed in Independently**
- **D- or T-type Flip-flops**
- **Product Term or Direct Input Pin Clocking**
- **Registered or Combinatorial Internal Feedback**
- **Backward Compatible with ATV2500B/BQL and ATV2500H/L Software**
- **Advanced Electrically-erasable Technology**
  - **Reprogrammable**
  - **100% Tested**
- **44-lead Surface Mount Package**

Block Diagram



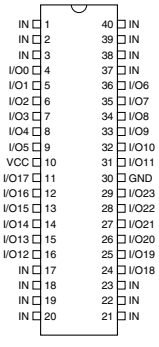
Description

The ATF2500C is the highest-density PLD available in a 44-pin package. With its fully connected logic array and flexible macrocell structure, high gate utilization is easily obtainable. The ATF2500C is a high-performance CMOS (electrically-erasable) programmable logic device (PLD) that utilizes Atmel's proven electrically-erasable technology. *(continued)*

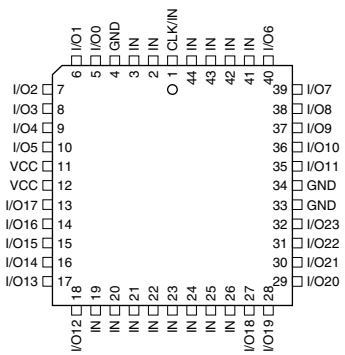
Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bi-directional Buffers
I/O 0,2,4...	"Even" I/O Buffers
I/O 1,3,5...	"Odd" I/O Buffers
GND	Ground
VCC	+5V Supply

DIP



PLCC/LCC/JLCC



Note: For ATF2500CQ and ATF2500CQL (PLCC/LCC packages) pin 4 and pin 26 GND connections are not required.

ATF2500C CPLD Family

ATF2500C
ATF2500CL
ATF2500CQ
ATF2500CQL

Preliminary

Rev. 0777E–04/01

The ATF2500C is organized around a single universal array. All pins and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

In the ATF2500C, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with no performance penalty. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

The Atmel-unique "L" low-power feature is an edge-sensing option that is now field programmable for the ATF2500C family. The "L" feature utilizes Atmel-patented Input Transition Detection (ITD) circuitry and is activated by selecting the "L" option from the program menu.

Using the ATF2500C Family's Many Advanced Features

The ATF2500Cs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATF2500Cs key features are:

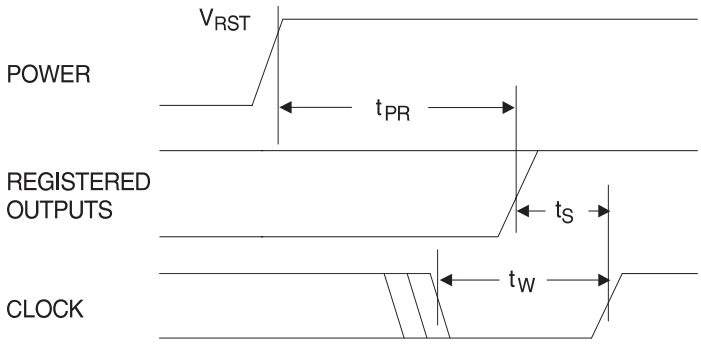
- **Fully Connected Logic Array –** Each array input is always available to every product term. This makes logic placement a breeze.
- **Selectable D- and T-Type Registers –** Each ATF2500C flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Buried Combinatorial Feedback –** Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.
- **Selectable Synchronous/Asynchronous Clocking –** Each of the ATF2500Cs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Total of 48 Registers –** The ATF2500C provides two flip-flops per macrocell – a total of 48. Each register has its own clock and reset terms, as well as its own sum term.
- **Independent I/O Pin and Feedback Paths –** Each I/O pin on the ATF2500C has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.
- **Combinable Sum Terms –** Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with *no speed penalty.*

Power-up Reset

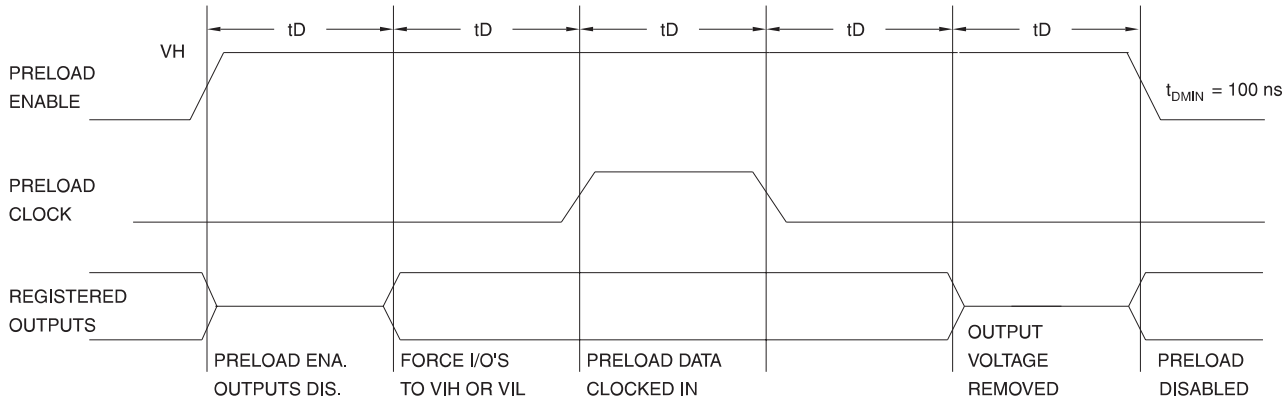
The registers in the ATF2500Cs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state as nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin or terms high, and
3. The clock pin, and any signals from which clock terms are derived, must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V



Level Forced on Odd I/O Pin during PRELOAD Cycle	Q Select Pin State	Even/Odd Select	Even Q1 State after Cycle	Even Q2 State after Cycle	Odd Q1 State after Cycle	Odd Q2 State after Cycle
V_{IH}/V_{IL}	Low	Low	High/Low	X	X	X
V_{IH}/V_{IL}	High	Low	X	High/Low	X	X
V_{IH}/V_{IL}	Low	High	X	X	High/Low	X
V_{IH}/V_{IL}	High	High	X	X	X	High/Low

Preload and Observability of Registered Outputs

The ATF2500Cs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 10.25V to 10.75V signal on SMP lead 42. When the preload clock SMP lead 23 is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 10.25V to 10.75V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.

Programming Software Support

As with all other Atmel PLDs, several third party PLD development software products and programmers will support the ATF2500Cs.

Additionally, the ATF2500C may be programmed to perform the ATV2500H/Ls functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H/L JEDEC file. In this case, the ATF2500C becomes a direct replacement or speed upgrade for the ATV2500H/L (additional GND connections are required). Please refer to the Programmable Logic Development Tools section for a complete PLD software and programmer listing.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of ATF2500C fuse patterns. Once programmed, the outputs will read programmed during verify.

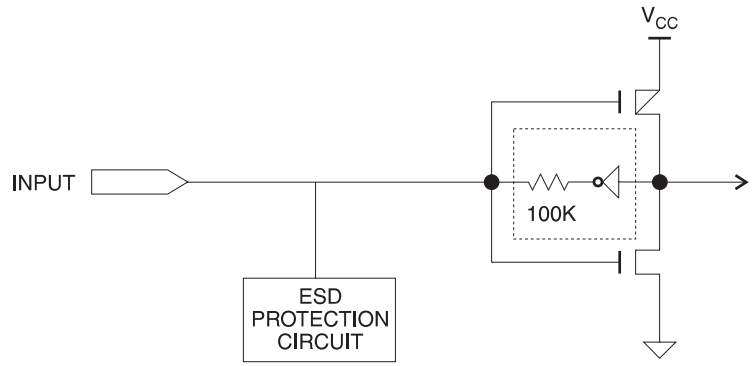
The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

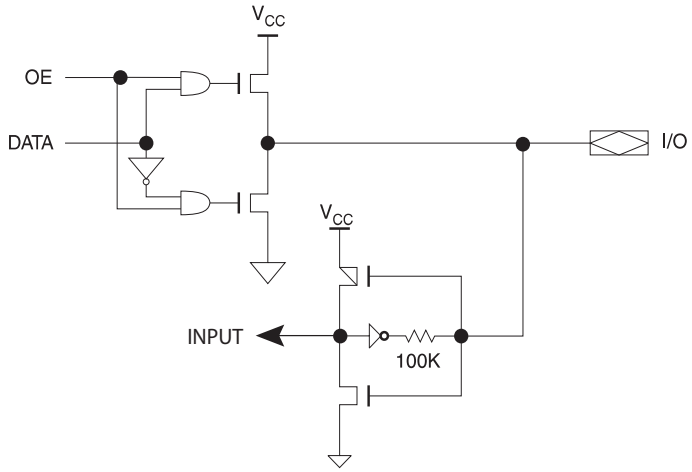
Input and I/O Pull-ups

All ATF2500C family members have programmable internal input and I/O pinkeeper circuits. When pinkeepers are active, inputs or I/Os not being driven externally will maintain their last driven state. This ensures that all logic array inputs and device outputs are known states. Pinkeepers are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The ATF2500C functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

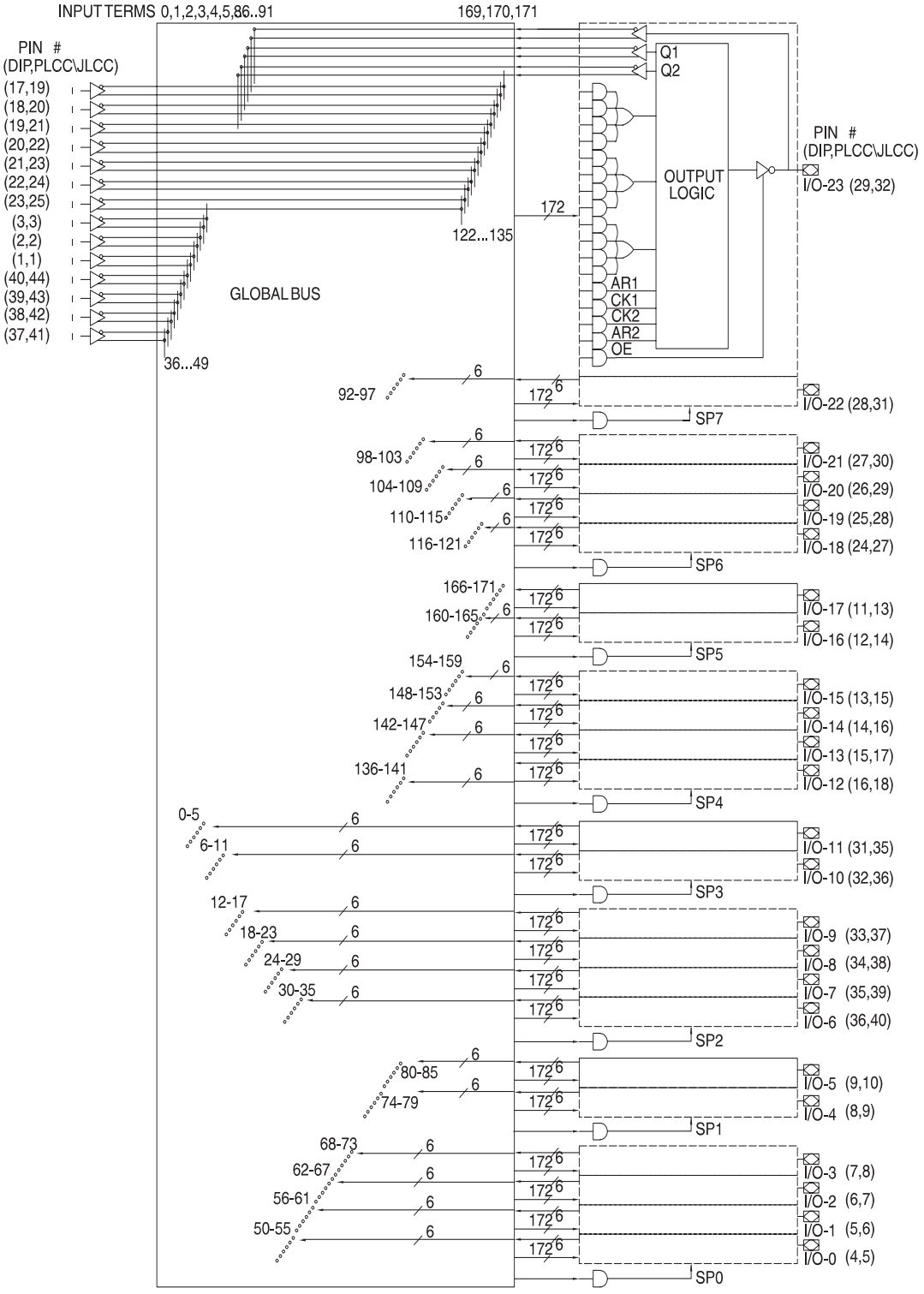
The ATF2500Cs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2[(1)] true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

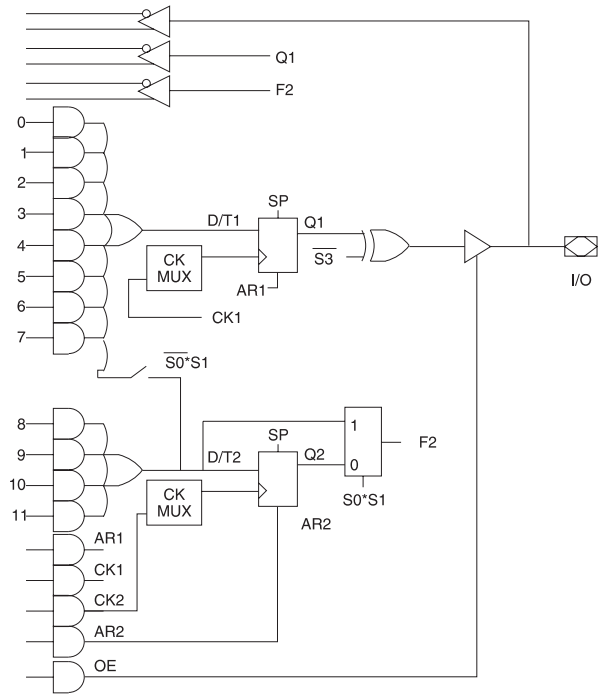
Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be fed back in the ATF2500Cs.

Functional Logic Diagram ATV2500C



Note: 1. Not required for PLCC versions of ATF2500CQ or ATF2500CQL, making them compatible with ATV2500H and ATV2500L as well as ATV2500BQ and ATV2500BQL pinouts.

Output Logic, Registered[1]



S2 = 0		Terms in		
S1	S0	D/T1	D/T2	Output Configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4[1]	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

S3	Output Configuration
0	Active Low
1	Active High

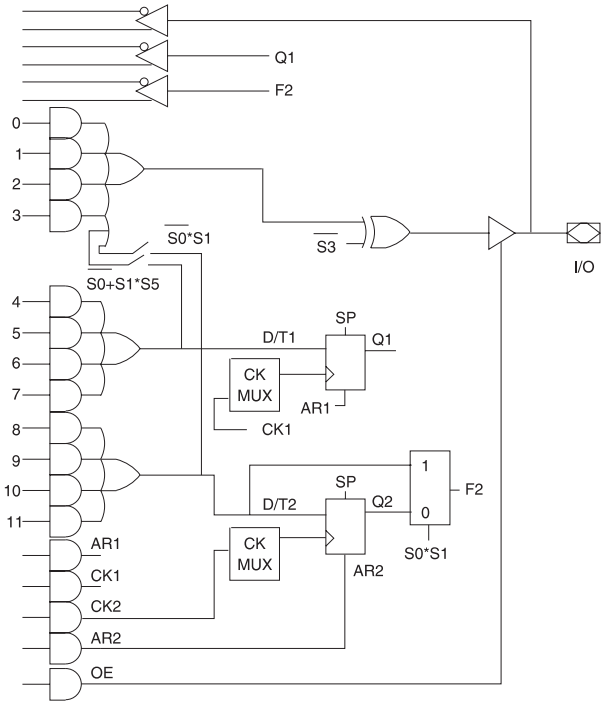
S4	Register 1 Type
0	D
1	T

S5	Register 2 Type
0	D
1	T

S6	Q1 CLOCK
0	CK1
1	CK1 • PIN1

S7	Q2 CLOCK
0	CK2
1	CK2 • PIN1

Output Logic, Combinatiorial[1]

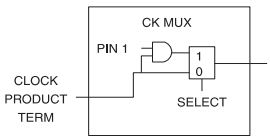


Note: 1. These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

S2 = 1			Terms in		
S5	S1	S0	D/T1	D/T2	Output Configuration
X	0	0	4[1]	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4[1]	4[1]	Combinatorial (12 Terms); Q2 FB
1	1	1	4[1]	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

Note: 1. These four terms are shared with D/T1.

Clock Option



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial	Military
Operating Temperature	0°C - 70°C (Ambient)	-40°C - 85°C (Ambient)	-55°C - 125°C (Case)
V_{CC} Power Supply	5V ± 5%	5V ± 10%	5V ± 10%

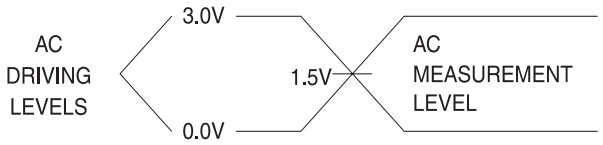
Pin Capacitance

f = 1 MHz, T = 25°C(1)

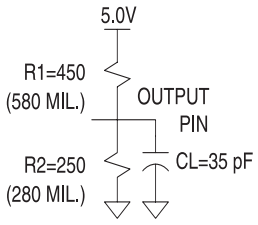
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

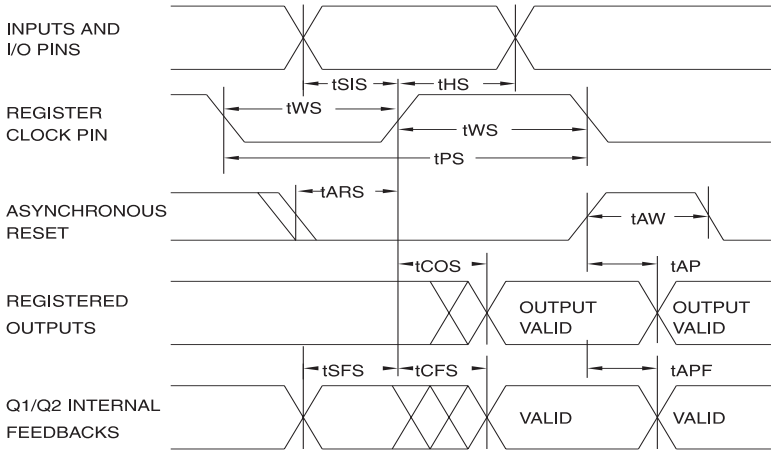
Input Test Waveforms and Measurement Levels



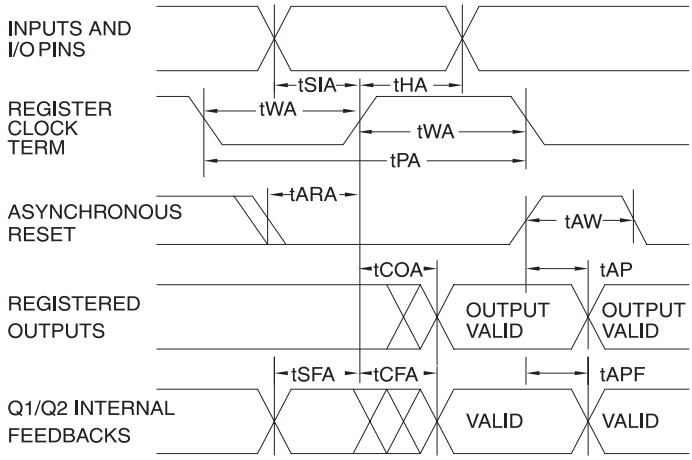
Output Test Load



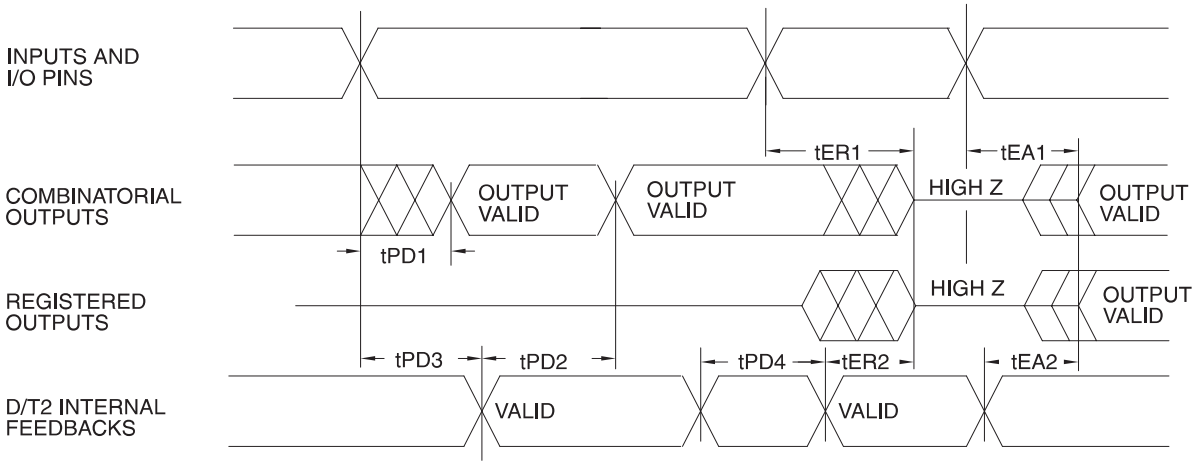
AC Waveforms[1] Input Pin Clock



AC Waveforms[1] Product Term Clock.



AC Waveforms[1] Combinatorial Outputs and Feedback



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified

ATF2500C DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATF2500C	Com.		110	190	mA
				Ind., Mil.		110	210	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	MIN ≤ V_{CC} ≤ MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5V	I_{OL} = 8 mA	Com., Ind.			0.5	V
			I_{OL} = 6 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			

Note: 1. See I_{CC} versus frequency characterization curves.

ATF2500C AC Characteristics

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		10		15	ns
t_{PD2}	Feedback to Non-registered Output		10		15	ns
t_{PD3}	Input to Non-registered Feedback		6		11	ns
t_{PD4}	Feedback to Non-registered Feedback		6		11	ns
t_{EA1}	Input to Output Enable		10		15	ns
t_{ER1}	Input to Output Disable		10		15	ns
t_{EA2}	Feedback to Output Enable		10		15	ns
t_{ER2}	Feedback to Output Disable		10		15	ns
t_{AW}	Asynchronous Reset Width	4		8		ns
t_{AP}	Asynchronous Reset to Registered Output		13		18	ns
t_{APF}	Asynchronous Reset to Registered Feedback		10		15	ns

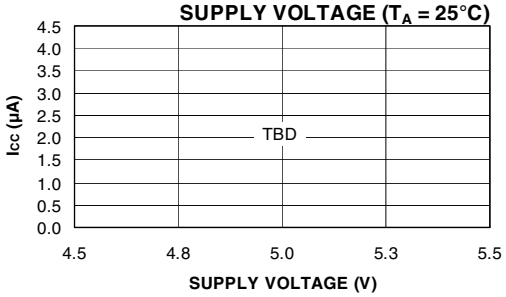
ATF2500C Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{COS}	Clock to Output		5.5		10	ns
t_{CFS}	Clock to Feedback	0	2	0	5	ns
t_{SIS}	Input Setup Time	2		9		ns
t_{SFS}	Feedback Setup Time	2		9		ns
t_{HS}	Hold Time	0		0		ns
t_{WS}	Clock Width	3		6		ns
t_{PS}	Clock Period	8		12		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		75		52	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		100		71	MHz
	No Feedback $1/(t_{PS})$		110		83	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	5		12		ns

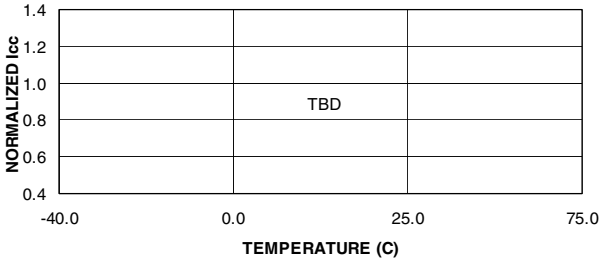
ATF2500C Register AC Characteristics, Product Term Clock

Symbol	Parameter	-10		-15		Units
		Min	Max	Min	Max	
t_{COA}	Clock to Output		10		15	ns
t_{CFA}	Clock to Feedback	2	5	5	12	ns
t_{SIA}	Input Setup Time	2		5		ns
t_{SFA}	Feedback Setup Time	2		5		ns
t_{HA}	Hold Time	1		5		ns
t_{WA}	Clock Width	3		7.5		ns
t_{PA}	Clock Period	9		15		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		75.5		50	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		100		58	MHz
	No Feedback $1/(t_{PS})$		100		66	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	2		8		ns

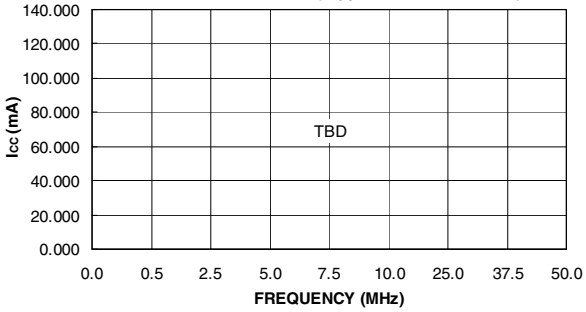
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



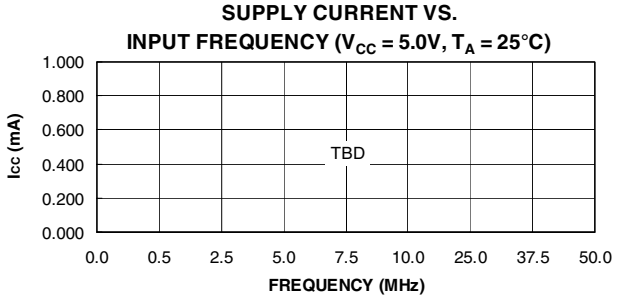
NORMALIZED I_{CC} VS. TEMP



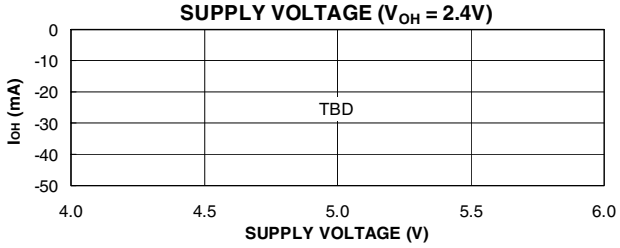
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



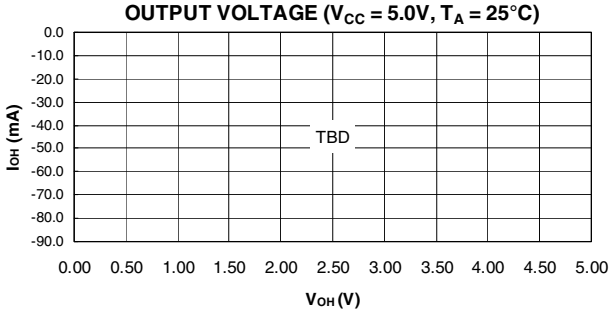
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



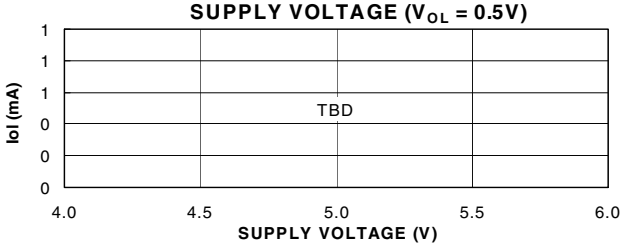
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



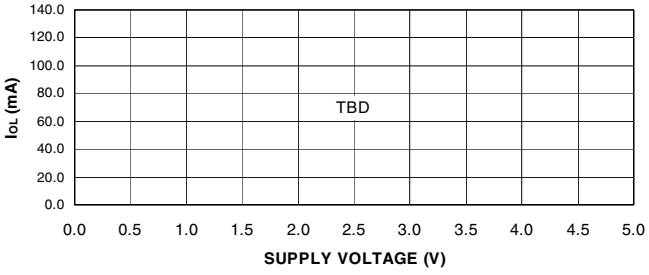
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



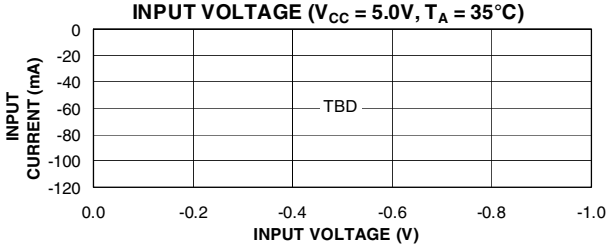
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



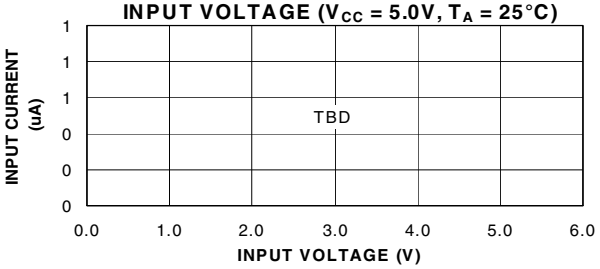
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



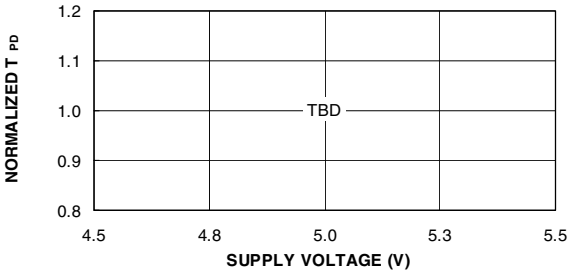
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



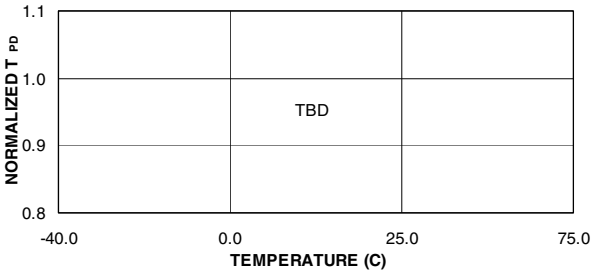
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



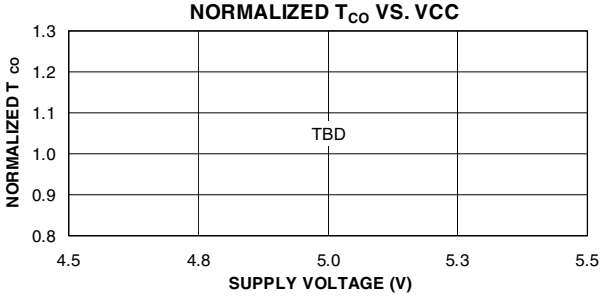
NORMALIZED T_{PD} VS. VCC



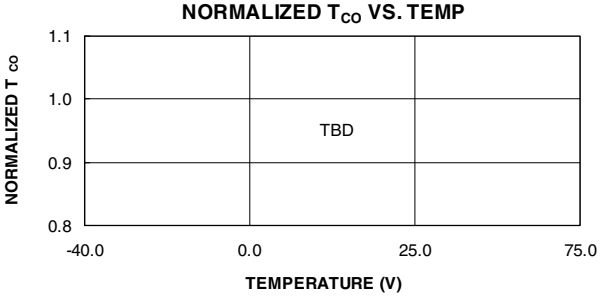
NORMALIZED T_{PD} VS. TEMP



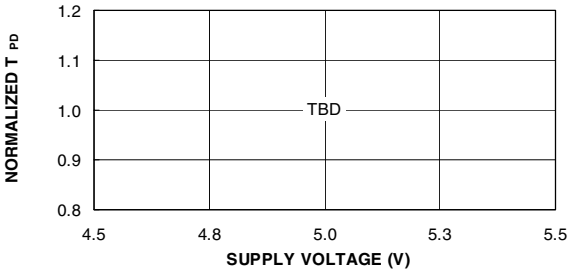
NORMALIZED T_{CO} VS. VCC



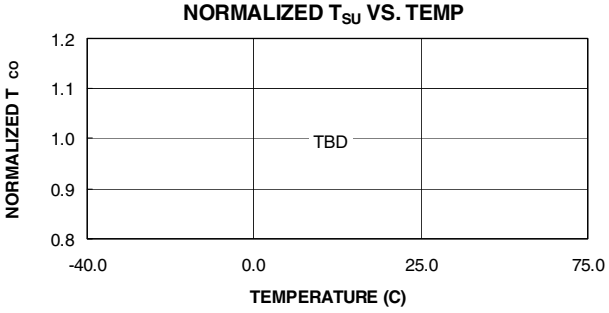
NORMALIZED T_{CO} VS. TEMP



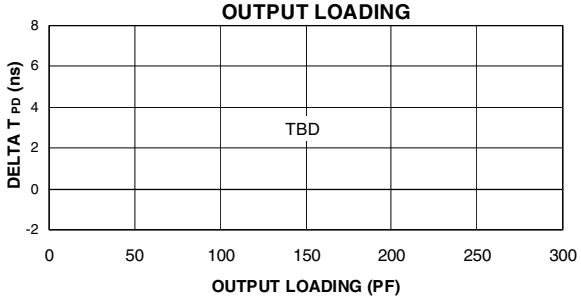
NORMALIZED T_{PD} VS. VCC



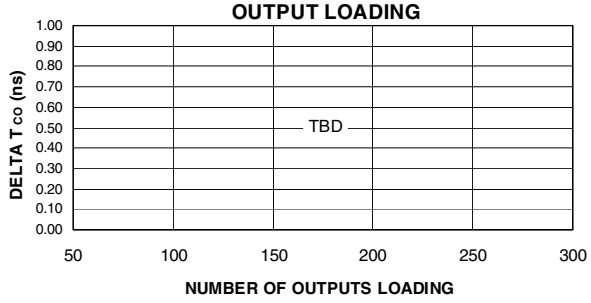
NORMALIZED T_{SU} VS. TEMP



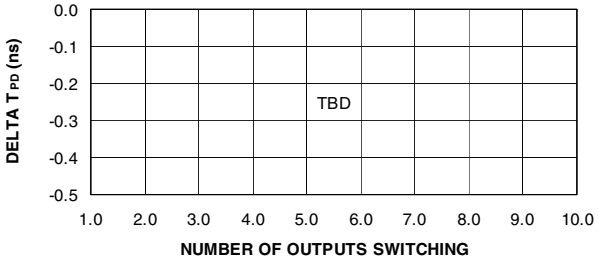
DELTA T_{PD} VS. OUTPUT LOADING



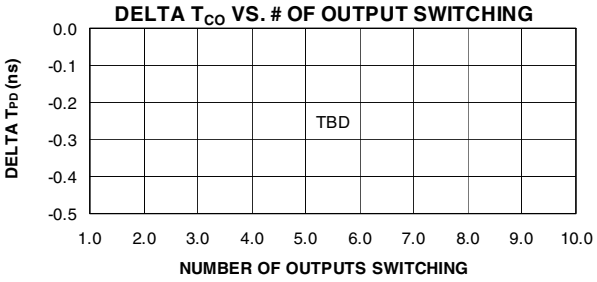
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF2500CL DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATF2500CL	Com.		2	5	mA
				Ind., Mil.		2	10	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	MIN ≤ V_{CC} ≤ MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5V	I_{OL} = 8 mA	Com., Ind.			0.5	V
			I_{OL} = 6 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			

Note: 1. See I_{CC} versus frequency characterization curves.

ATF2500CL AC Characteristics

Symbol	Parameter	-20		Units
		Min	Max	
t_{PD1}	Input to Non-registered Output		20	ns
t_{PD2}	Feedback to Non-registered Output		20	ns
t_{PD3}	Input to Non-registered Feedback		15	ns
t_{PD4}	Feedback to Non-registered Feedback		15	ns
t_{EA1}	Input to Output Enable		20	ns
t_{ER1}	Input to Output Disable		20	ns
t_{EA2}	Feedback to Output Enable		20	ns
t_{ER2}	Feedback to Output Disable		20	ns
t_{AW}	Asynchronous Reset Width	12		ns
t_{AP}	Asynchronous Reset to Registered Output		22	ns
t_{APF}	Asynchronous Reset to Registered Feedback		19	ns

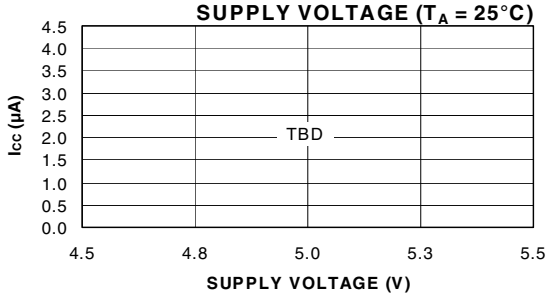
ATF2500CL Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-20		Units
		Min	Max	
t_{COS}	Clock to Output		11	ns
t_{CFS}	Clock to Feedback	0	6	ns
t_{SIS}	Input Setup Time	14		ns
t_{SFS}	Feedback Setup Time	14		ns
t_{HS}	Hold Time	0		ns
t_{WS}	Clock Width	7		ns
t_{PS}	Clock Period	14		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		40	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		50	MHz
	No Feedback $1/(t_{PS})$		71	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	15		ns

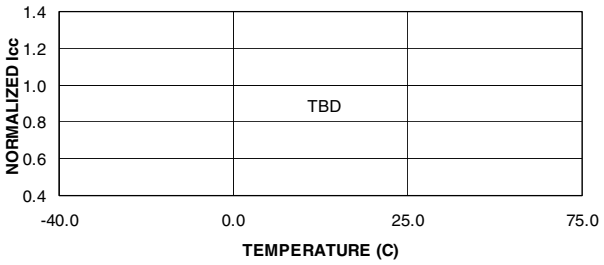
ATF2500CL Register AC Characteristics, Product Term Clock

Symbol	Parameter	-20		Units
		Min	Max	
t_{COA}	Clock to Output		20	ns
t_{CFA}	Clock to Feedback	10	16	ns
t_{SIA}	Input Setup Time	10		ns
t_{SFA}	Feedback Setup Time	8		ns
t_{HA}	Hold Time	10		ns
t_{WA}	Clock Width	11		ns
t_{PA}	Clock Period	22		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		33	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		38	MHz
	No Feedback $1/(t_{PS})$		45	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	12		ns

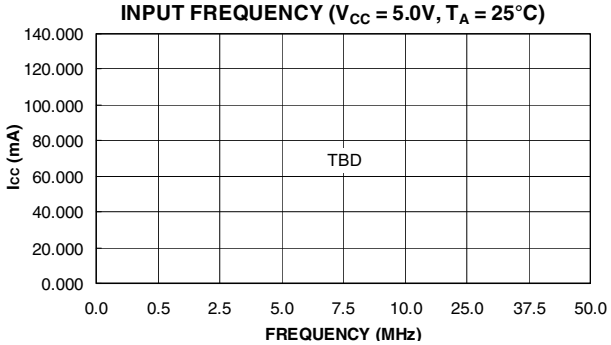
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



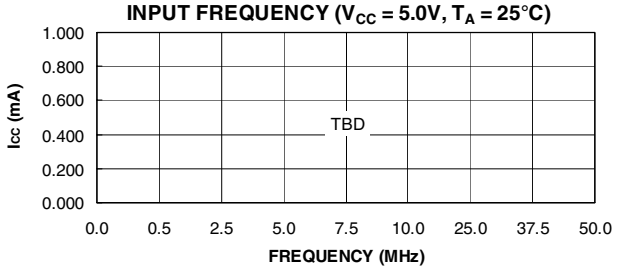
NORMALIZED I_{CC} VS. TEMP



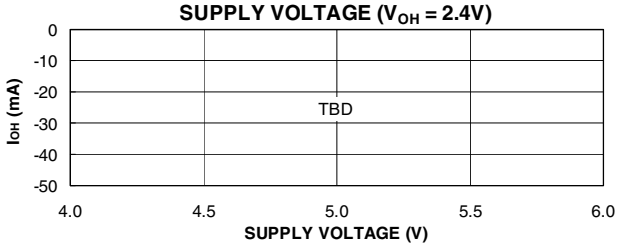
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



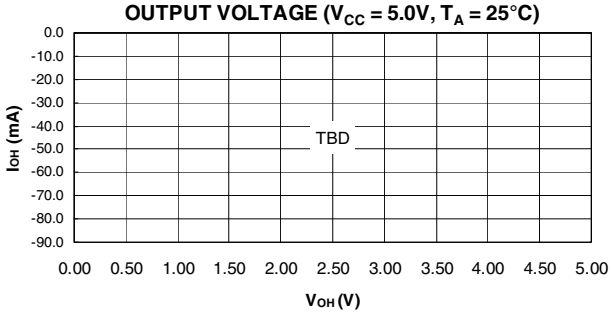
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



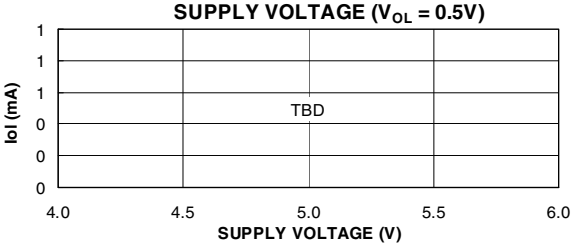
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



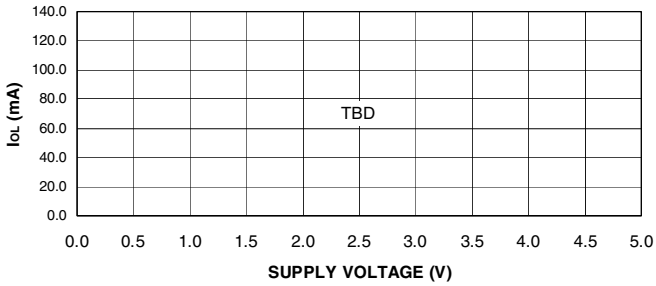
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



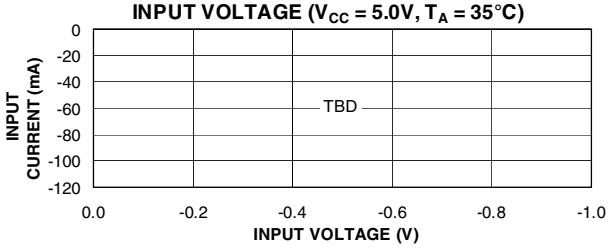
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



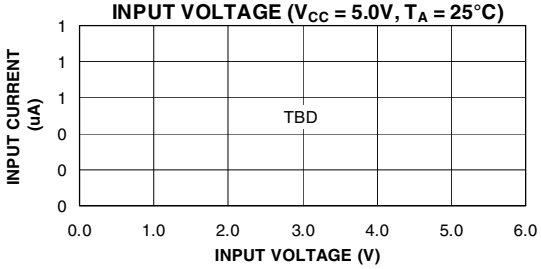
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



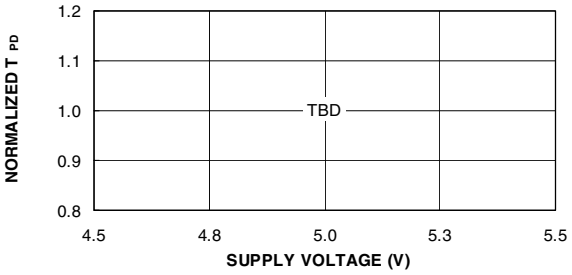
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



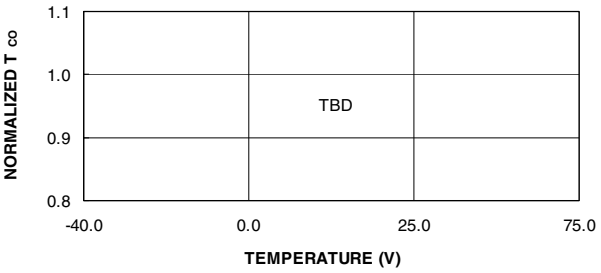
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



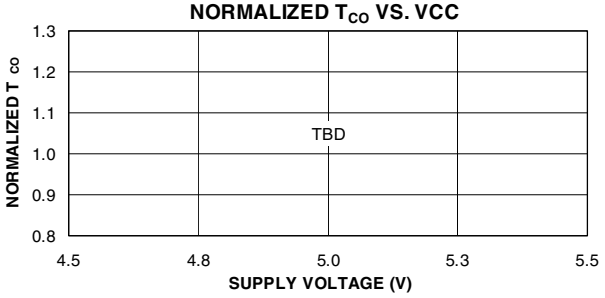
NORMALIZED T_{PD} VS. VCC



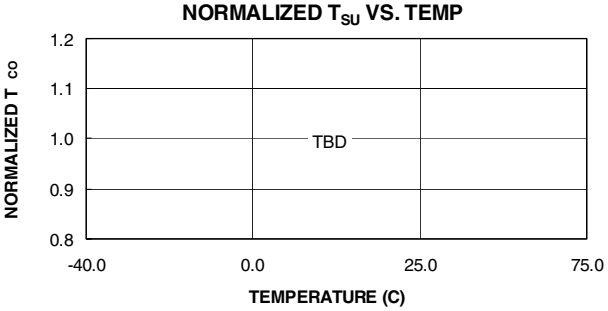
NORMALIZED T_{CO} VS. TEMP



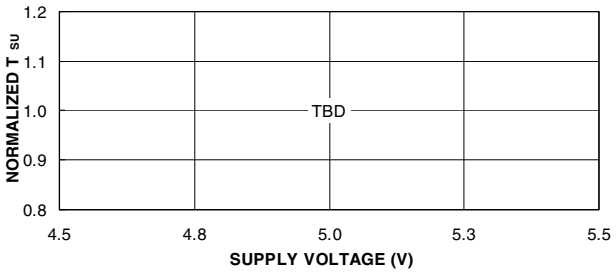
NORMALIZED T_{CO} VS. VCC



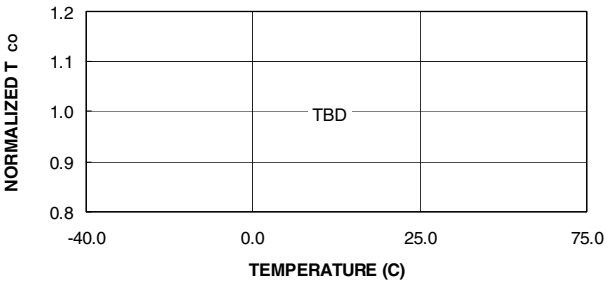
NORMALIZED T_{SU} VS. TEMP



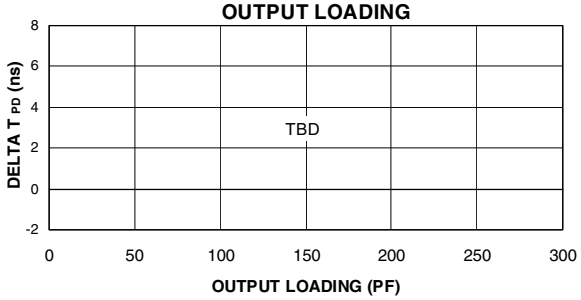
NORMALIZED T_{SU} VS. VCC



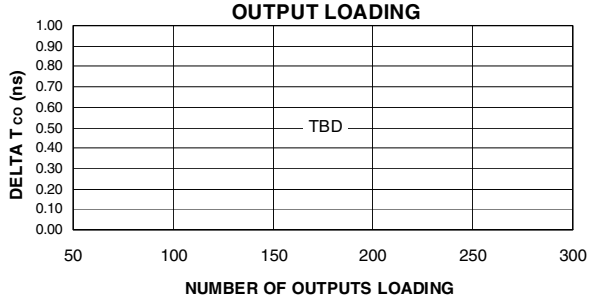
NORMALIZED T_{SU} VS. TEMP



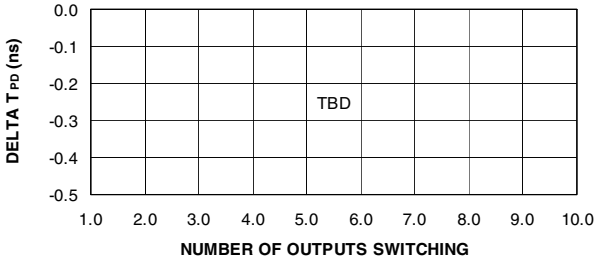
DELTA T_{PD} VS. OUTPUT LOADING



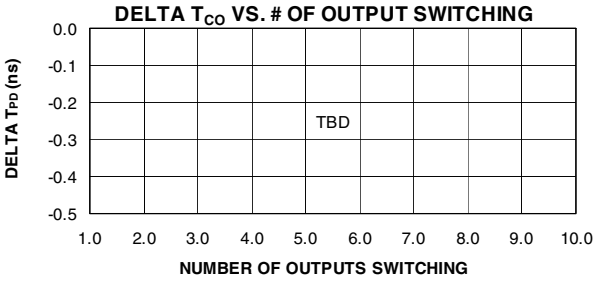
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF2500CQ DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATF2500CQ	Com.		30	70	mA
				Ind., Mil.		30	85	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	MIN ≤ V_{CC} ≤ MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5V	I_{OL} = 8 mA	Com., Ind.			0.5	V
			I_{OL} = 6 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			

Note: 1. See I_{CC} versus frequency characterization curves.

ATF2500CQ AC Characteristics

Symbol	Parameter	-20		-25		Units
		Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		20		25	ns
t_{PD2}	Feedback to Non-registered Output		20		25	ns
t_{PD3}	Input to Non-registered Feedback		15		18	ns
t_{PD4}	Feedback to Non-registered Feedback		15		18	ns
t_{EA1}	Input to Output Enable		20		25	ns
t_{ER1}	Input to Output Disable		20		25	ns
t_{EA2}	Feedback to Output Enable		20		25	ns
t_{ER2}	Feedback to Output Disable		20		25	ns
t_{AW}	Asynchronous Reset Width	12		15		ns
t_{AP}	Asynchronous Reset to Registered Output		22		28	ns
t_{APF}	Asynchronous Reset to Registered Feedback		19		25	ns

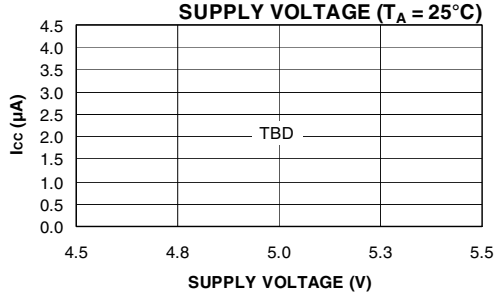
ATF2500CQ Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-20		-25		Units
		Min	Max			
t_{COS}	Clock to Output		11		12	ns
t_{CFS}	Clock to Feedback	0	6	0	7	ns
t_{SIS}	Input Setup Time	14		20		ns
t_{SFS}	Feedback Setup Time	14		20		ns
t_{HS}	Hold Time	0		0		ns
t_{WS}	Clock Width	7		8		ns
t_{PS}	Clock Period	14		16		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		40		31	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		50		37	MHz
	No Feedback $1/(t_{PS})$		71		62	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	15		20		ns

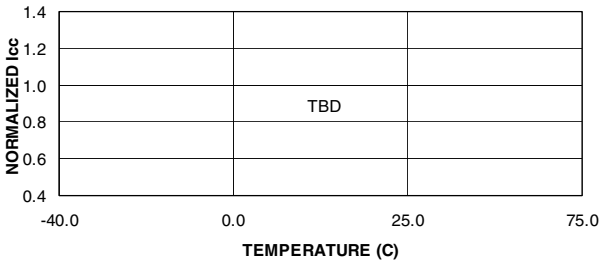
ATF2500CQ Register AC Characteristics, Product Term Clock

Symbol	Parameter	-20		-25		Units
		Min	Max			
t_{COA}	Clock to Output		20		22	ns
t_{CFA}	Clock to Feedback	10	16	12	18	ns
t_{SIA}	Input Setup Time	10		15		ns
t_{SFA}	Feedback Setup Time	8		10		ns
t_{HA}	Hold Time	10		12		ns
t_{WA}	Clock Width	11		14		ns
t_{PA}	Clock Period	22		28		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		33		27	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		38		36	MHz
	No Feedback $1/(t_{PS})$		45		36	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	12		15		ns

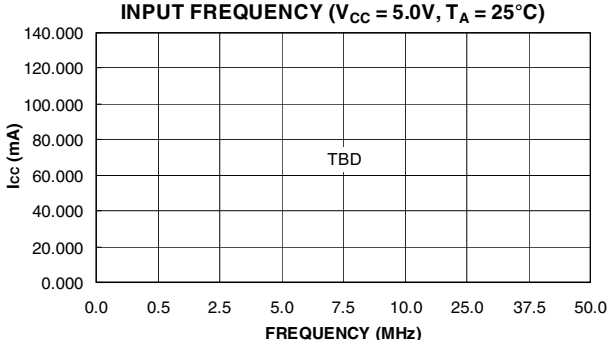
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



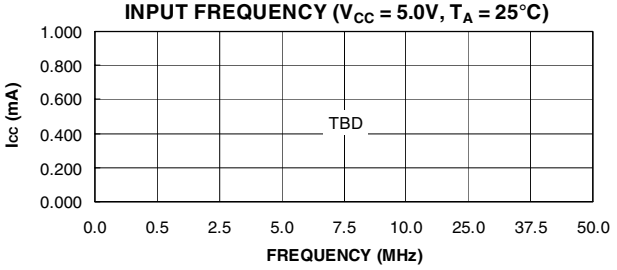
NORMALIZED I_{CC} VS. TEMP



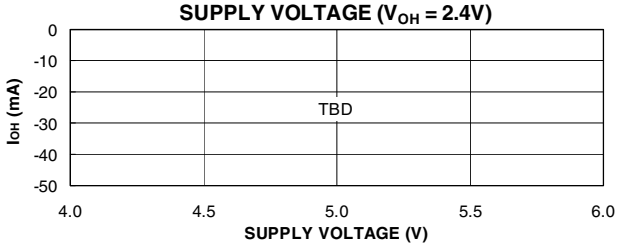
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



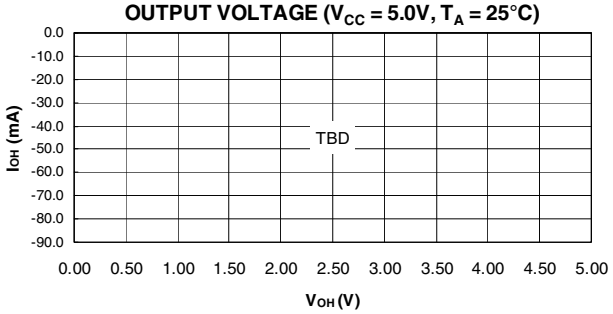
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



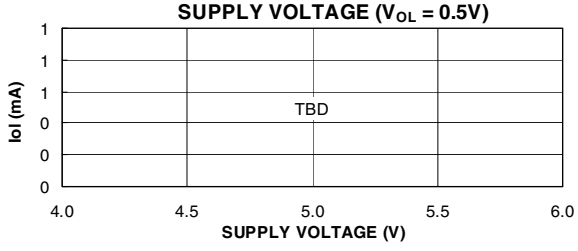
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



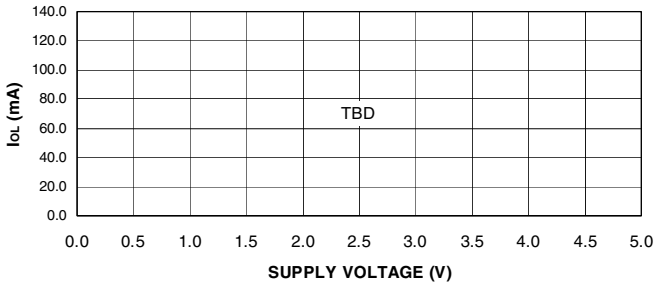
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



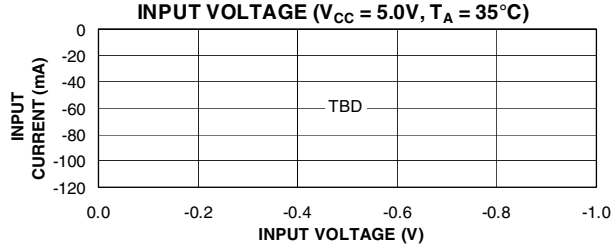
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



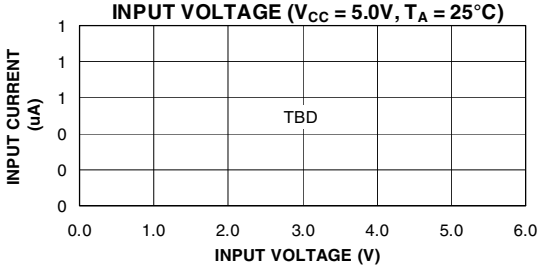
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



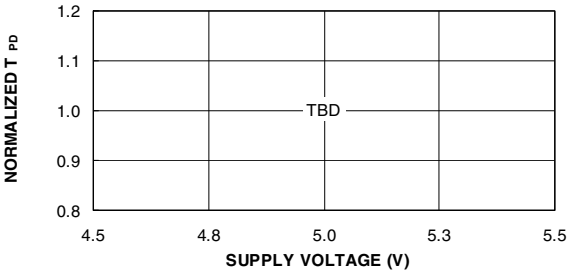
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



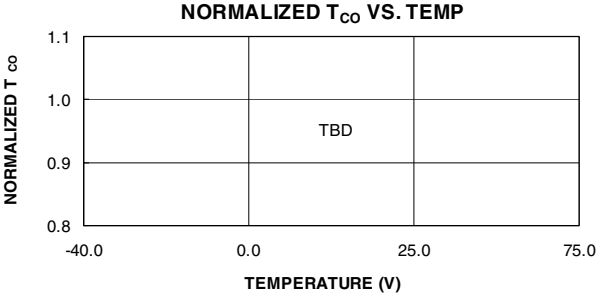
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



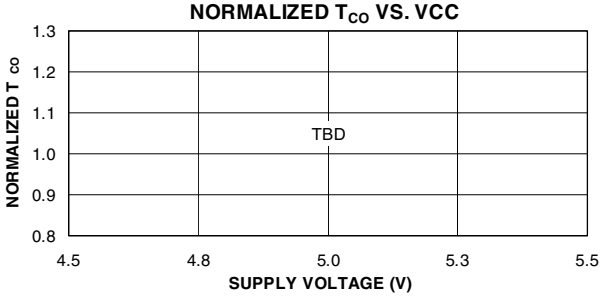
NORMALIZED T_{PD} VS. VCC



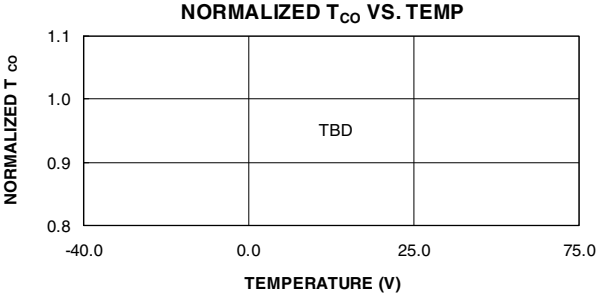
NORMALIZED T_{CO} VS. TEMP



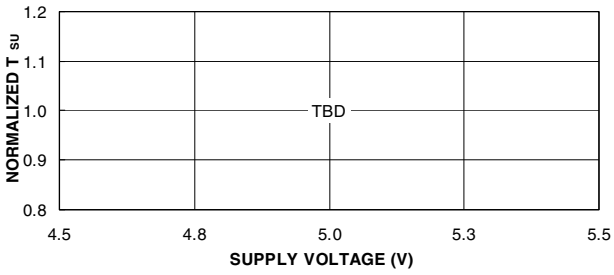
NORMALIZED T_{CO} VS. VCC



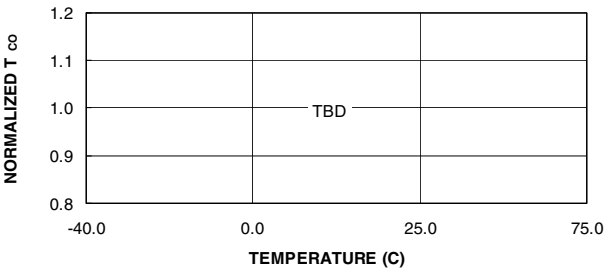
NORMALIZED T_{CO} VS. TEMP



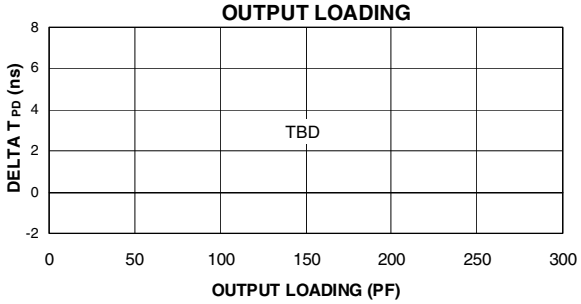
NORMALIZED T_{SU} VS. VCC



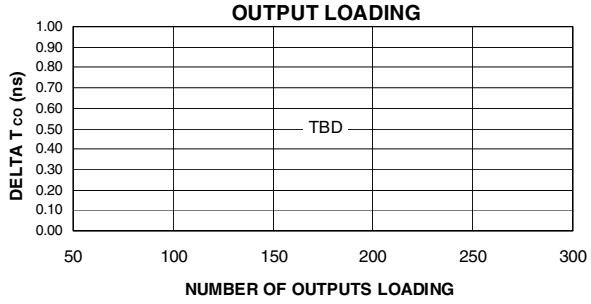
NORMALIZED T_{SU} VS. TEMP



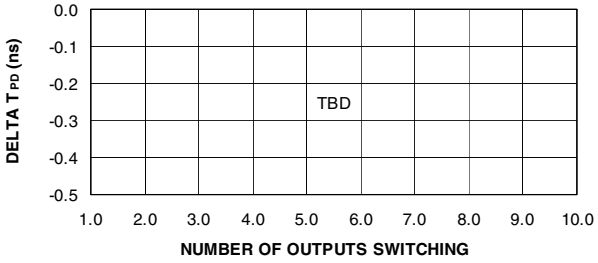
DELTA T_{PD} VS. OUTPUT LOADING



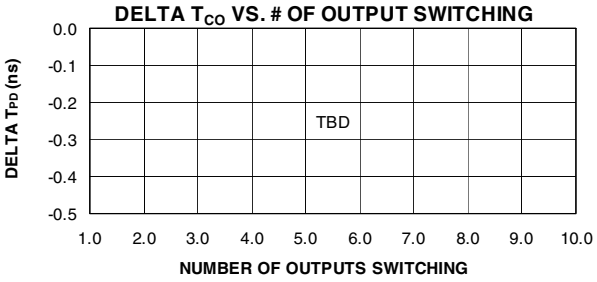
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF2500CQL DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATF2500CQL	Com.		2	4	mA
				Ind., Mil.		2	5	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	MIN ≤ V_{CC} ≤ MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5V	I_{OL} = 8 mA	Com., Ind.			0.5	V
			I_{OL} = 6 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			

Note: 1. See I_{CC} versus frequency characterization curves.

ATF2500CQL AC Characteristics

Symbol	Parameter	-25		-30		Units
		Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		25		30	ns
t_{PD2}	Feedback to Non-registered Output		25		30	ns
t_{PD3}	Input to Non-registered Feedback		18		20	ns
t_{PD4}	Feedback to Non-registered Feedback		18		20	ns
t_{EA1}	Input to Output Enable		25		30	ns
t_{ER1}	Input to Output Disable		25		30	ns
t_{EA2}	Feedback to Output Enable		25		30	ns
t_{ER2}	Feedback to Output Disable		25		30	ns
t_{AW}	Asynchronous Reset Width	15		18		ns
t_{AP}	Asynchronous Reset to Registered Output		28		30	ns
t_{APF}	Asynchronous Reset to Registered Feedback		25		30	ns

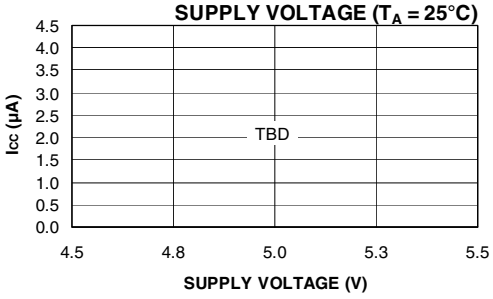
ATF2500CQL Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-25		-30		Units
		Min	Max	Min	Max	
t_{COS}	Clock to Output		12		15	ns
t_{CFS}	Clock to Feedback	0	7	0	8	ns
t_{SIS}	Input Setup Time	20		23		ns
t_{SFS}	Feedback Setup Time	20		23		ns
t_{HS}	Hold Time	0		0		ns
t_{WS}	Clock Width	8		9		ns
t_{PS}	Clock Period	146		18		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		31		26	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		37		32	MHz
	No Feedback $1/(t_{PS})$		62		55	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		ns

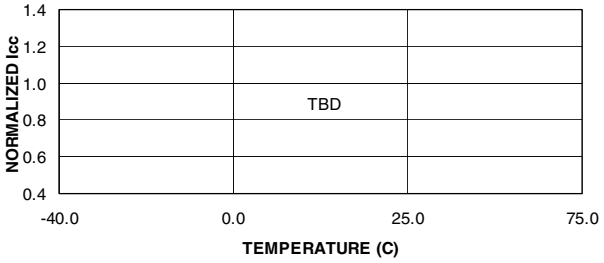
ATF2500CQL Register AC Characteristics, Product Term Clock

Symbol	Parameter	-25		-30		Units
		Min	Max	Min	Max	
t_{COA}	Clock to Output		22		25	ns
t_{CFA}	Clock to Feedback	12	18	13	20	ns
t_{SIA}	Input Setup Time	15		19		ns
t_{SFA}	Feedback Setup Time	10		10		ns
t_{HA}	Hold Time	12		13		ns
t_{WA}	Clock Width	14		15		ns
t_{PA}	Clock Period	28		30		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		27		23	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		36		24	MHz
	No Feedback $1/(t_{PS})$		36		33	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		18		ns

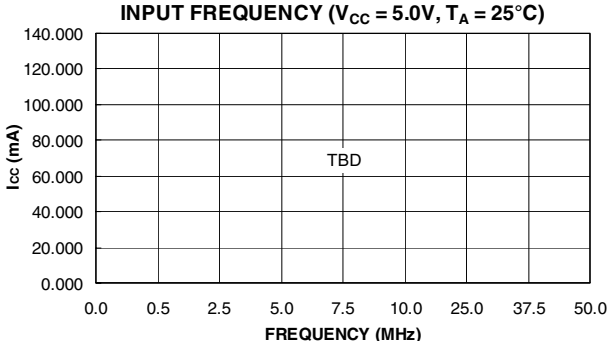
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



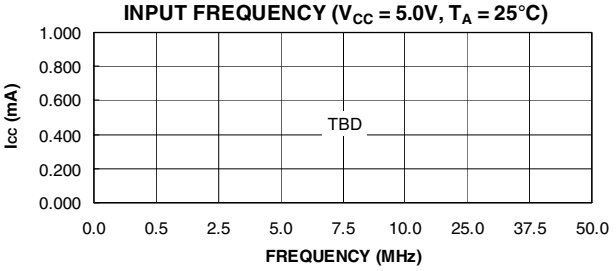
NORMALIZED I_{CC} VS. TEMP



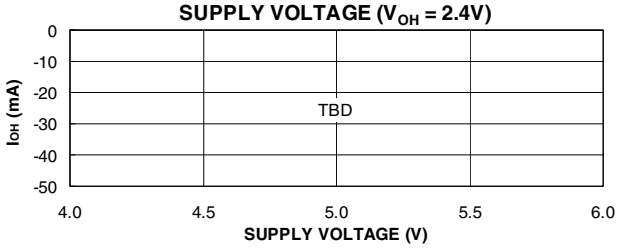
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



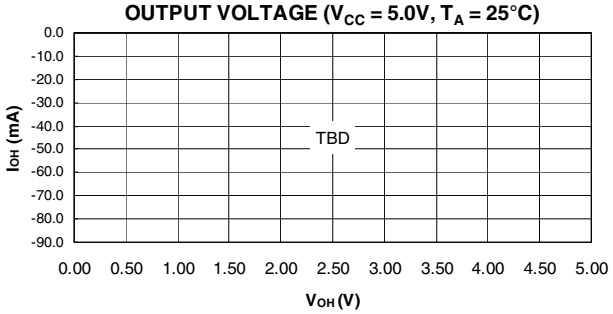
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



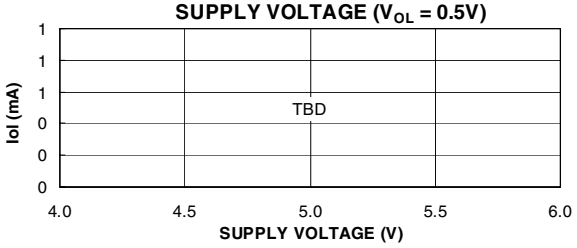
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



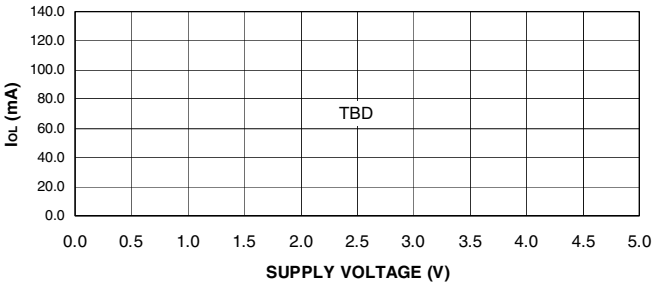
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



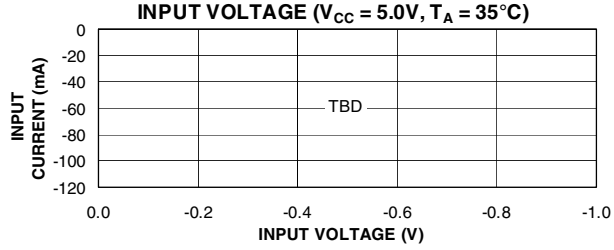
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



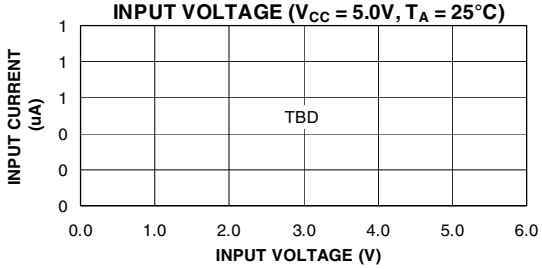
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



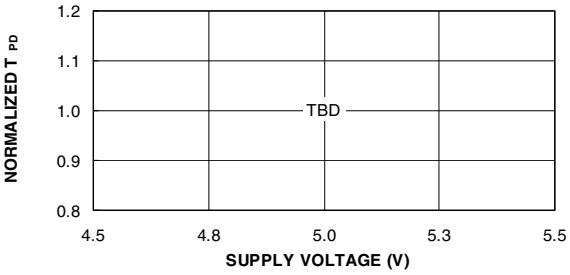
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



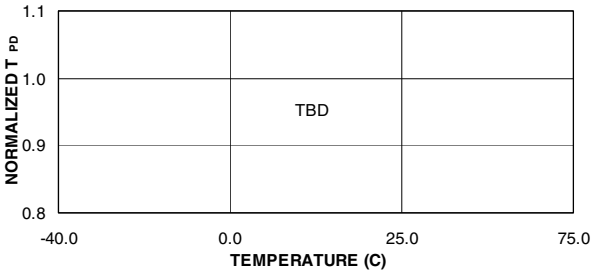
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



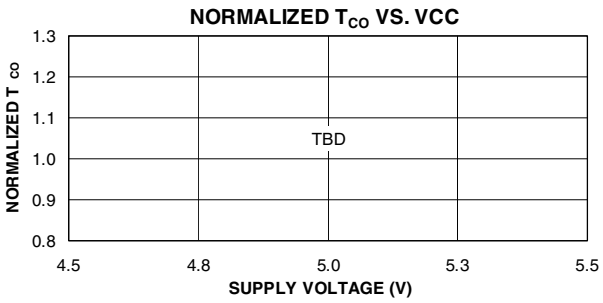
NORMALIZED T_{PD} VS. VCC



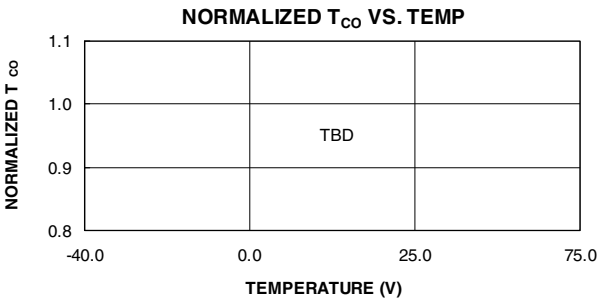
NORMALIZED T_{PD} VS. TEMP



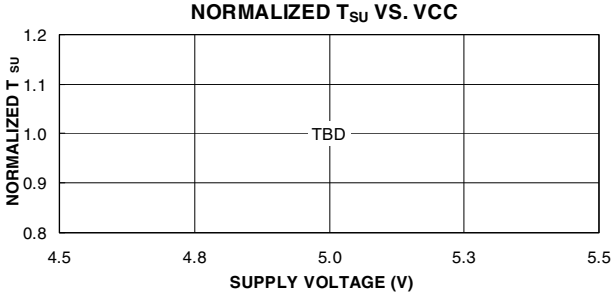
NORMALIZED T_{CO} VS. VCC



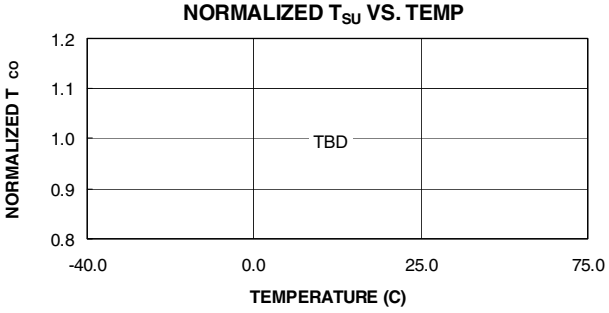
NORMALIZED T_{CO} VS. TEMP

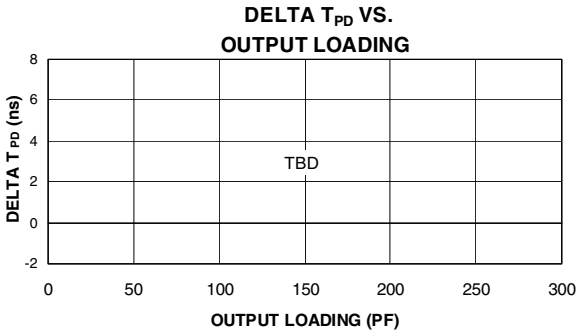


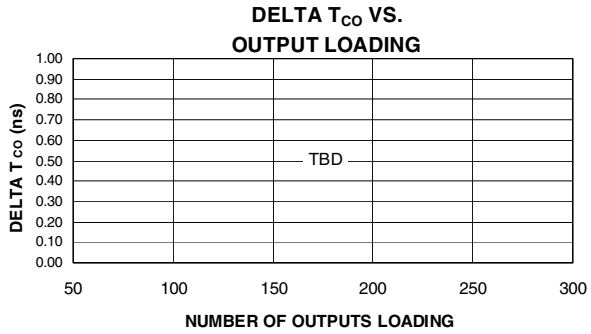
NORMALIZED T_{SU} VS. VCC

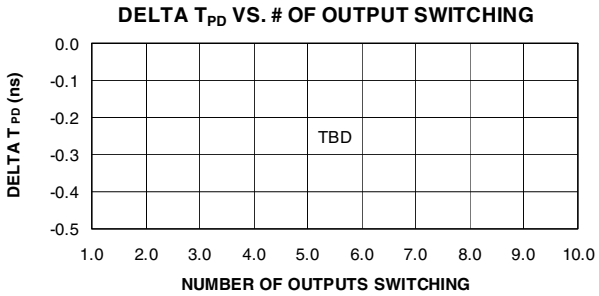


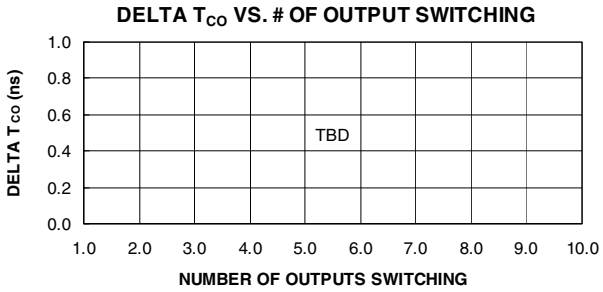
NORMALIZED T_{SU} VS. TEMP




DELTA T_{PD} VS.
OUTPUT LOADING
DELTA T_{PD} (ns)
8
6
4
2
0
-2
TBD
0
50
100
150
200
250
300
OUTPUT LOADING (PF)


DELTA T_{CO} VS.
OUTPUT LOADING
DELTA T_{CO} (ns)
1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
TBD
50
100
150
200
250
300
NUMBER OF OUTPUTS LOADING


DELTA T_{PD} VS. # OF OUTPUT SWITCHING
DELTA T_{PD} (ns)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING


DELTA T_{CO} VS. # OF OUTPUT SWITCHING
DELTA T_{CO} (ns)
1.0
0.8
0.6
0.4
0.2
0.0
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
12	7.5	69	ATF2500C-10JC ATF2500C-10KC	44J 44K	Commercial (0°C to 70°C)
15	10	52	ATF2500C-15JC ATF2500C-15KC	44J 44K	Commercial (0°C to 70°C)
			ATF2500C-15JI ATF2500C-15KI	44J 44K	Industrial (-40°C to 85°C)
			ATF2500C-15KM ATF2500C-15NM	44K 44L	Military (-55°C to 125°C)
			ATF2500C-15KM/883 ATF2500C-15NM/883	44K 44L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATF2500CL-20JC ATF2500CL-20KC	44J 44K	Commercial (0°C to 70°C)
			ATF2500CL-20KM ATF2500CL-20NM	44K 44L	Military (-55°C to 125°C)
			ATF2500CL-20KM/883 ATF2500CL-20NM/883	44K 44L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATF2500CQ-20GC ATF2500CQ-20JC ATF2500CQ-20KC ATF2500CQ-20PC	40D6 44J 44K 40P6	Commercial (0°C to 70°C)
25	12	31	ATF2500CQ-25GC ATF2500CQ-25JC ATF2500CQ-25KC ATF2500CQ-25PC	40D6 44J 44K 40P6	Commercial (0°C to 70°C)
			ATF2500CQ-25GI ATF2500CQ-25JI ATF2500CQ-25KI ATF2500CQ-25PI	40D6 44J 44K 40P6	Industrial (-40°C to 85°C)
			ATF2500CQ-25GM ATF2500CQ-25KM ATF2500CQ-25NM	40D6 44K 44L	Military/883C (-55°C to 125°C)
			ATF2500CQ-25GM/883 ATF2500CQ-25KM/883 ATF2500CQ-25NM/883	40D6 44K 44L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	ATF2500CQL-25GC ATF2500CQL-25JC ATF2500CQL-25KC ATF2500CQL-25PC	40D6 44J 44K 40P6	Commercial (0°C to 70°C)
25	12	31	ATF2500CQL-25GI ATF2500CQL-25JI ATF2500CQL-25KI ATF2500CQL-25PI	40D6 44J 44K 40P6	Industrial (-40°C to 85°C)

Ordering Information (Continued)

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
30	15	26	ATF2500CQL-30GM ATF2500CQL-30KM ATF2500CQL-30NM	40D6 44K 44L	Military/883C (-55°C to 125°C)
	15	26	ATF2500CQL-30GM/883 ATF2500CQL-30KM/883 ATF2500CQL-30NM/883	40D6 44K 44L	Military/883C (-55°C to 125°C) Class B. Fully Compliant
15	10	52	5962 - * 5962 - *	44L 44K	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	5962 - * 5962 - *	44L 44K	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	5962 - * 5962 - * 5962 - *	44L 44K 40D6	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	26	5962 - * 5962 - * 5962 - *	44L 44K 40D6	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Note: * SMD numbers are TBD.

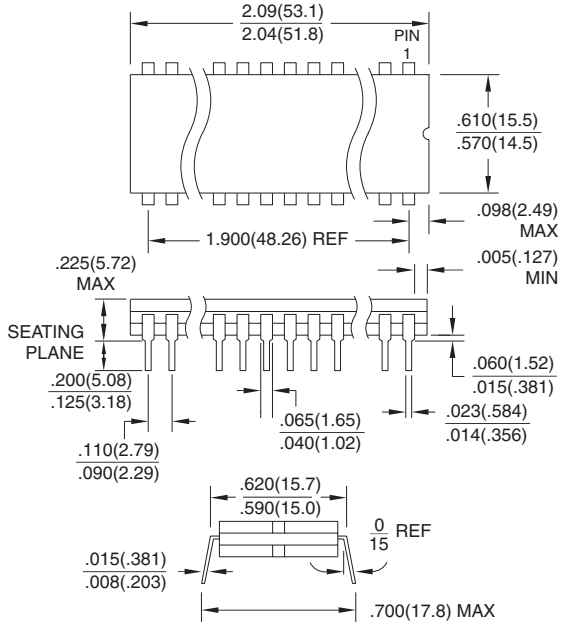
Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

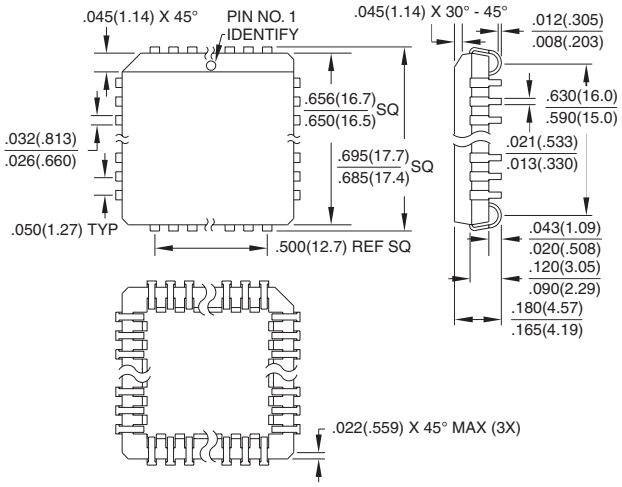
Package Type	
40D	40-pin, 0.600" Wide, Ceramic, Dual Inline Package (Cerdip)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
44K	44-lead, Ceramic J-leaded Chip Carrier (JLCC)
40P6	40-pin, 0.600" Wide, Plastic, Dual Inline Package OTP (PDIP)
44L	44-pad, Ceramic Leadless Chip Carrier (LCC)

Packaging Information

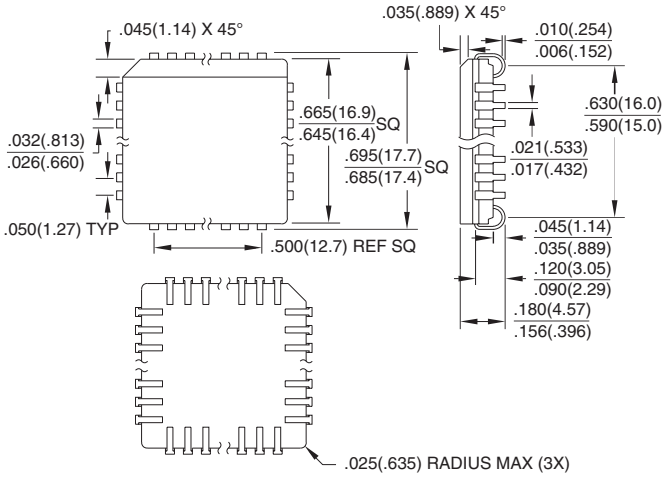
40D6, 40-lead, 0.600” Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



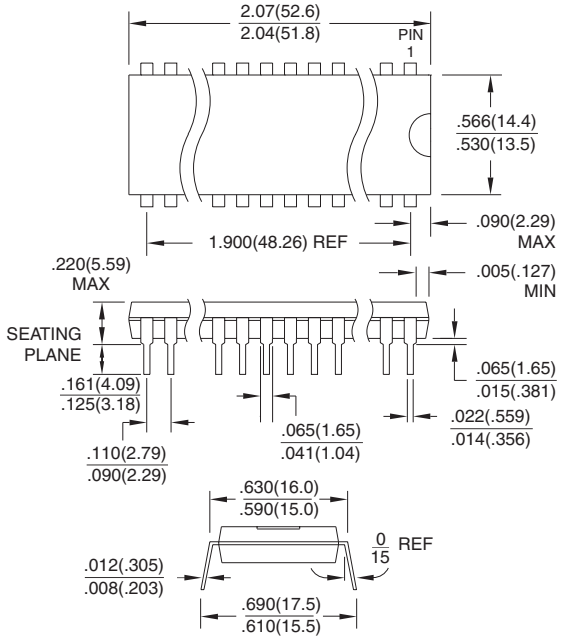
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



44K, 44-lead, Non-windowed, Ceramic J-leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)

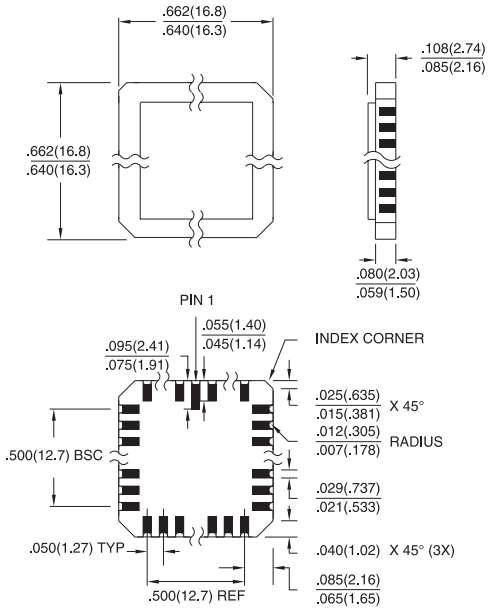


40P6, 40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDED STANDARD MS-011 AC



Packaging Information

44L, 44-pad, 0.600” Wide, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-5



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